ABSTRACT

ENHANCED SHALLOW TRENCH ISOLATION (STI) METHOD FOR FABRICATING RADIATION-TOLERANT INTEGRATED CIRCUIT DEVICES

An enhanced shallow trench isolation method for fabricating radiation tolerant integrated circuit devices is disclosed. A layer of pad oxide is first deposited on a semiconductor substrate. A layer of pad nitride is then deposited on the pad oxide layer. A trench is defined within the semiconductor substrate by selectively etching the pad nitride layer, the pad oxide layer, and the semiconductor substrate. Boron ions are then implanted into both the bottom and along the sidewalls of the trench. Subsequently, a trench plug is formed within the trench by depositing an insulating material into the trench and by removing an excess portion of the insulating material. A p-well is implanted to a depth just below the depth of the bottom of the trench. This helps to keep the threshold voltage of the IC device below the trench at a high level, and thereby keep post-radiation leakage low. Then, an electrically neutral species is implanted into the wafer.

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